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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,504	06/22/2001	Douglas Deao	TI-30100	7710

7590 05/20/2004

EXAMINER	
CHAVIS, JOHN Q	

ART UNIT	PAPER NUMBER
2124	

Robert L. Troike
Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,504	DEAO ET AL.	
	Examiner	Art Unit	
	John Chavis	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Proteat et al. (5,970,245).

Claims:	Proteat
1. In a data exchange system for transferring data between a host processor and a target processor comprising	See the title and abstract and col. 2 lines 35-47, which indicates that multiple targets are present and furthermore indicates that the DLL's may be received from one or more communication devices (target) coupled to the computer (host).
a data unit on said target processor that transfers said data from said target processor to an emulator and a device driver on said host processor that transfers data from said emulator,	
a system for dynamically linking and loading emulation software support for a new target processor comprising:	See the DLL, which is resolved at runtime, col. 3 lines 13-23. The trace

	procedures perform the emulation functions, via its one to one correspondence with the target DLL, col. 2 lines 48-64.
a target interface module for the host computer that supports the new target processor kind; and	The target DLL provides the target interface module for the host.
a target interface module for the emulator that supports the new target processor kind.	The trace DLL provides the Target emulator that supports the new target.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Proteat as applied to claim 1 above, and further in view of choice of selecting a specific debug link and a specific communication module.

Claims	Proteat
2. A method for at time of use linking and loading of emulation software for one or more debuggers on a host computer to communicate with a mix of target processors via a JTAG debug link and emulator comprising the steps of: connecting a debugger for each processor to a target interface for that kind of processor; determining if there is support for that kind	The features of this claim are indicated above. The only feature that is not taught is the feature of utilizing a JTAG debug link; however, it is noted that this feature is not defined in the specifications and therefore the feature is considered to

of processor in the emulator by the target interface communicating with a dynamic loader on the host computer; if not support loading a target interface into the emulator and connecting to an already running emulation software on the host computer; and connecting the target interface software on the emulator to the target interface software on the host computer.	have been well known in the art at the time of the invention to ensure enablement for the applicant's invention. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to Utilize a specific debug link in Proteat's system, since it is clear that some type of link is required to connect the two systems to ensure proper communication between the systems implementing different targets. Also, the DLL feature inherently provides for determining and loading features. Note also that specific DLL's are selectively linked (if not support loading...), col. 4 lines 21-63.
3. The method of claim 2 wherein said steps are repeated for each debugger, for each kind of processor on the target **system.**	See col. 3 line 59-col. 4 line 5.
4. The method of claim 2 wherein said determining step includes communicating using ECOM modules on the host computer and emulator over a host computer to emulator connection.	The ECOM modules are also not specifically taught by Proteat; however, again it is clear that some type of Functions (modules) are provided for Proteat's system and therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize specific functions (ECOM modules) in Proteat's system since the

overall functionality of the system remains the same regardless of which specific modules are used and it is clear that the applicant merely selected specific modules to use; since, they are also not defined in the specifications.

5. A system for at time of use linking and loading of emulation software for one or more debuggers on a host computer to communicate with a mix of target processors via a JTAG debug link and emulator comprising:

a debugger for each processor connected to a target interface for that type of processor;

means for determining if there is support for that type of processor in the emulator by communicating with a dynamic loader on the host computer; means if there is no support for loading a target interface into the emulator

and connecting to an already running emulation software on the host computer; and

means for providing a connection to the target interface on the emulator to the target interface software on the host computer.

See the rejection of claim 2.

6. The system of claim 3 wherein a single debugger can support more than one kind of processor and

including a system description file stored on the host computer describes a particular mix of processors to be supported and said debugger reads the system description to determine which kinds of target interfaces are required for operation and

then it communicates with each required target interface to establish connection.

These features are inherent in the features of claims 2.

7. In combination: a single debugger that can support more than one processor or kind of processor; a system description file stored on a host computer describes the particular mix of processors to be supported; said debugger reads this system description to determine which kinds of target interfaces are required for operation and then communicates with each required target interface to establish connection to the target system.	See again the rejection of claim 2 above.
8. The combination of claim 7 wherein said debugger determines if there is support for that kind of processor in the emulator by the target interface communicating with a dynamic loader on the host computer; if not support loads a target interface into the emulator and connects to an already running emulation software on the host computer; and connects the target interface software on the emulator to the target interface software on the host computer.	See the rejection of claim 2.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Chavis whose telephone number is (703) 305-9665. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jqc
May 13, 2004

John Chavis
Patent Examiner (AU-2124)